BY EXPRESS MAIL NO. EL254109412US
Attorney Docket KOIK-P9501
09/462342
426 Rec'd PCT/PTO 07 JAN 2000

22 pgs

DESCRIPTION

Apparatus and Method for Transmitting Information,

Apparatus and Method for Receiving Information,

Apparatus and Method for Transmitting and Receiving Information, and

Recording Medium

Technical Field

This invention relates to an apparatus and method for transmitting information, an apparatus and method for receiving information, an apparatus and method for transmitting and receiving information, and a recording medium. More particularly, the invention relates to an apparatus and method for transmitting information, an apparatus and method for receiving information, an apparatus and method for transmitting and receiving information, and a recording medium, all for use in communicating information with reference to a mapping table that describes the correlation among a plurality buses including IEEE1394 serial data buses.

Background Art

Recently, not only character information, but also high-definition still images, moving images, voice and sound, which are large items of information, are transmitted in Internet. For example, the so-called "Inter-net TV telephone" has been realized, in which voice and images are communicated in real time.

The amount of information transferred through Internet has increased as mentioned above. In addition, Internet users have fast increased in numbers. As a

consequence, the communication lines (Internet lines) are congested, lengthening the time for accessing the servers and a part of the information is lost in the course of communication.

The architecture of Internet was devised about 20 years ago. Thus, the ATM (Asynchronous Transfer Mode) technique, i.e., a high-speed data communication technique developed through the recent technical advance, cannot be efficiently in Internet.

Disclosure of the Invention

This invention has been made in view of the foregoing. It is the object of the invention is to inhibit loss of information in the course of communication and to accomplish high-speed information communication by the use of the ATM technique.

That is, the object of the invention is to provide an apparatus and method for transmitting information and a recording medium, all designed to inhibit loss of information in the course of communication and to accomplish high-speed information communication by the use of the ATM technique.

Another object of this invention is to provide an apparatus and method for receiving information and a recording medium, all designed to inhibit loss of information in the course of communication.

Still another object of the invention is to provide an apparatus and method for transmitting and receiving information and a recording medium, all designed to inhibit loss of information in the course of communication and to accomplish high-speed

information communication by the use of the ATM technique.

Another object of this invention is to provide an apparatus and method for receiving information and a recording medium, all capable of receiving data in real time, among different networks that use asynchronous clock signals.

In the present invention, information is transmitted in the band of the second network reserved, with reference to a mapping table, thereby to inhibit loss of the information while the information is being transmitted and also to achieve high-speed transmission of the information by the use of the ATM technique.

Further, information is transmitted in the band of the reserved network, with reference to the mapping table, whereby loss of the information can be inhibited while the information is being transmitted, and high-speed communication of the information can be performed by the use of the ATM technique. Still further, the time data contained in a packet is altered in accordance with the time lug between the first and second clock signals, thereby make it possible for different network, which use asynchronous clock signals, to receive data from one another in real time.

That is, according to the present invention there is provided an information transmitting apparatus for use in a first network, designed to transmit information via a second network to an information receiving apparatus that is incorporated in a third network. The information transmitting apparatus is characterized by comprising band-reserving means for reserving a band for the second network; generating means for generating a mapping table showing the address of the information-receiving

apparatus; and transmitting means for transmitting information by referring to the mapping table generated by the generating means.

According to the invention, there is provided a method of transmitting information in an apparatus for use in a first network, designed to transmit information via a second network to an information receiving apparatus incorporated in a third network. The method is characterized by comprising: a band-reserving step of reserving a band for the second network; a generating step of generating a mapping table showing the address of the information-receiving apparatus, and a transmitting step of transmitting information by referring to the mapping table generated in the generating step.

According to this invention there is provided recording medium recording a program for use in a first network, designed to perform a process of transmitting information via a second network to an information receiving apparatus incorporated in a third network. The recording medium is characterized in that said program can be executed by a computer and includes: a band-reserving step of reserving a band for the second network; a generating step of generating a mapping table showing the address of the information-receiving apparatus, and a transmitting step of transmitting information by referring to the mapping table generated in the generating step.

According to the present invention, there is provided an information receiving apparatus for use in a first network, designed to receive information via a second network from an information transmitting apparatus incorporated in a third network.

The information receiving apparatus is characterized by comprising generating means for generating a mapping table showing the address of the information transmitting apparatus; and transfer means for transferring information by referring to the mapping table generated by the generating means.

According to the invention there is provided method of receiving information in an information receiving apparatus for use in a first network, designed to receive information via a second network from an information transmitting apparatus incorporated in a third network. The method is characterized by comprising; a generating step of generating a mapping table showing the address of the information transmitting apparatus; and a step of transferring information by referring to the mapping table generated in the generating step.

According to this invention there is provided a recording medium recording a program for use in a first network, designed to perform a process of receiving information via a second network from an information transmitting apparatus incorporated in a third network. The recording medium is characterized in that said program can be executed by a computer and includes: a generating step of generating a mapping table showing the address of the information transmitting apparatus; and a step of transferring information by referring to the mapping table generated in the generating step.

According to the present invention, there is provided an information transmitting/receiving apparatus for transmitting and receiving information through

a plurality of networks. The apparatus is characterized by comprising: reserving means for reserving bands for the networks; generating means for generating a mapping table showing the address of a destination; communicating means for communicating information by referring to the mapping table generated by the generating means; receiving means for receiving video information input; and GUI-generating means for generating a GUI, synthesizing the GUI with the video information received by the receiving means and outputting a combination of the GUI and the video information.

According to the invention, there is provided a method of transmitting and receiving information in an information transmitting/receiving apparatus for transmitting and receiving information through a plurality of networks. The method is characterized by comprising: a reserving step of reserving bands for the networks; a generating step of generating a mapping table showing the address of a destination; a communicating step of communicating information by referring to the mapping table generated in the generating step; a receiving step of receiving video information input; and a GUI-generating step of generating a GUI, synthesizing the GUI with the video information received in the receiving step and outputting a combination of the GUI and the video information.

According to this invention, there is provided a recording medium recording a program for use in an information transmitting/receiving apparatus for transmitting and receiving information through a plurality of networks. The recording medium is characterized in that said program can be executed by a computer and includes: a

reserving step of reserving bands for the networks; a generating step of generating a mapping table showing the address of a destination; a communicating step of communicating information by referring to the mapping table generated in the generating step; a receiving step of receiving video information input; and a GUI-generating step of generating a GUI, synthesizing the GUI with the video information received in the receiving step and outputting a combination of the GUI and the video information.

According to the invention there is provided an information receiving apparatus for use in a second network which operates in accordance with a second clock signal, designed to receive a packet transmitted from an information transmitting apparatus incorporated in a first network which operates in accordance with a first clock signal. The information receiving apparatus is characterized by comprising: receiving means for receiving the packet transmitted; detecting means for detecting a lag between the first clock signal and second signal used in the first network and the second network, respectively, on the basis of the packet received by the receiving means; changing means for changing time information contained in the packet, in accordance with the lag detected by the detecting means; and output means for outputting the packet received by the receiving means, in accordance with the time information changed by the changing means.

According to the present invention, there is provided a method of receiving information in an information receiving apparatus used in a second network which

09452350 - 040900

operates in accordance with a second clock signal, designed to receive a packet transmitted from an information transmitting apparatus incorporated in a first network which operates in accordance with a first clock signal, characterized by comprising: a receiving step of receiving the packet transmitted; a detecting step of detecting a lag between the first clock signal and second signal used in the first network and the second network, respectively, on the basis of the packet received in the receiving step; a changing step of changing time information contained in the packet, in accordance with the lag detected in the detecting step; and an outputting step of outputting the packet received in the receiving step, in accordance with the time information changed in the changing step.

Brief Description of the Drawings

FIG. 1 is a diagram illustrating a network system that has upward compatibility to the conventional Internet;

FIG. 2 is a block diagram showing the configuration of the TV telephone system to which the present invention is applied;

FIG. 3 is a block diagram depicting the connection between the translator incorporated in the TV telephone system and another apparatus;

FIG. 4 is a block diagram showing the connection between the controller provided in the TV telephone system and another apparatus;

FIG. 5 is a block diagram of a home router that comprises the translator and controller combined together;

FIG. 6 is a diagram explaining how the home router in the TV telephone system performs data communication;

FIG. 7 is a diagram explaining the data communication performed by the home router;

FIG. 8 is a diagram explaining the data communication performed by the home router;

FIG. 9 is a diagram explaining the GUI displayed on the monitor of the TV telephone system;

FIGS. 10A and 10B are diagrams explaining the GUI displayed on the monitor;

FIGS. 11A and 11B are diagrams explaining the GUI displayed on the monitor;

FIGS. 12A and 12B are diagrams explaining the GUI displayed on the monitor;

FIG. 13 is a diagram showing the setting input window displayed on the monitor;

FIGS. 14A, 14B and 14C are a flow chart explaining the GUI procedure in the TV telephone system;

FIG. 15 is a flow chart explaining the receiving step in the GUI procedure;

FIG. 16 is a flow chart explaining how the home router modifies the rate;

FIG. 17 is a diagram for explaining the format of a packet having a time stamp:

FIG. 18 is a diagram for explaining the format of a packet having no time stamps:

FIG. 19 is a flow chart explaining, in detail, the step of inserting a packet to be

executed in the step of modifying the rate, into an isochronous cue in order to add its data to the data to be transmitted; and

FIG. 20 is a diagram explaining the format of an empty packet.

Best Mode For Carrying Out the Invention

The best mode for carrying out the present invention will now be described with reference to the accompanying drawings.

First, a network system (hereinafter called "first network") that has upward compatibility to the conventional Internet will be explained. The first network is the next-generation network architecture that solves the problems with the existing network architecture. The first network is featured with high-speed resource- reserving protocol technique and application-oriented transfer protocol technique (rate control technique).

The high-speed resource- reserving protocol technique is to reserve at high speed a band (communication resource) for the line before data is transferred, thereby to transmit data without being interfered with other communication. This technique makes effective use of the quality-assurance network technology for the connection base, which characterizes the asynchronous transfer mode (ATM). With this technique it is possible to send data reliably to the transfer destination, because the data is transmitted after the route to the destination is determined. In the high-speed resource-reserving protocol technique, the band is reserved for the required time only, and the reservation is canceled once the data has been transferred. Hence, the band can be

used efficiently.

On the other hand, the application-oriented transfer protocol technique (rate control technique) is designed to use effectively the band secured by the high-speed resource- reserving protocol technique, without wasting time. It is the technique of calculating the transfer rate from the width of the band secured (reserved) before the data is transmitted, and then transmitting the data at the rate thus calculated.

The configuration of the first network 1 will be described, with reference to FIG. 1. In the first network 1, the edge routers 2-1 and 2-2 bundle the lines extending from the home routers of user terminals (networks of households and companies), and connect them to the backbone routers 3-1 to 3-3. The backbone routers 3-1 to 3-3 are connected to one another by optical fibers to transfer data by using the high-speed resource-reserving protocol technique and the application-oriented transfer protocol technique, both mentioned above.

A home router 4 is provided to connect the first network 1 to an IEEE1394 bus 5 (and also to terminal networks which are Ether nets). To this network there are connected a DVCR (Digital Video Cassette Recorder) 7, a digital video (DV) camera 8, and a monitor 6. The DVCR 7 has an IEEE1394 interface. The digital video camera 8 converts video data and audio data to DV data.

FIG. 2 illustrates the configuration of a TV telephone system to which the present invention is applied and which incorporates the system shown in FIG. 1. In this specification, the word "system" means an apparatus that comprises a plurality of

devices, a plurality of means, and the like.

A translator 10-1 and a controller 11-1 constitute a home router 4-1. The translator 10-1 may be a general-purpose personal computer. As shown in FIG. 3, the translator 10-1 is connected to the controller 11-1 by a 10-base T cable 16-1 that is connected to an Ether card 12. In response to a command supplied from the controller 11-1, the translator 10-1 transmits data to, or receives data from, the first network 1 through an optical fiber cable 1501 that is connected to an ATM card 22. The translator 10-1 converts the IP (Internet Protocol) data supplied from the first network 1, to DV data. The DV data is output to the DV terminal 25 of a DVCR 7-1 through a specific channel of an IEEE1394 bus 5-1-1. The translator 10-1 receives DV data (video data and audio data) input from a DV camera 8-1 via a specific channel of an IEEE1394 bus 5-1-2 connected to an IEEE1394 card 21, converts the DV data to IP data, and transmits the IP data to the first network 1. Further, the translator 10-1 controls the operation of the DVCR 7-1 and DV camera 8-1 by way of the IEEE1394 buses 5-1-1 and 5-1-2.

The controller 11-1 may be a general-purpose personal computer, too. As shown in FIG. 4, the controller 11-1 generates a GUI (Graphical User Interface) which the monitor 6-1 will display. The controller 11-1 supplies the GUI, in the form of an NTSC signal, to the input terminal A of the DVCR 7-1 via the S-video cable 17-1 connected to a video card 33, as is illustrated in FIG. 4. The controller 11-1 receives the video data supplied from the output terminal B of the DVCR 7-1 through the

S-video cable 18-1 connected to a capture card 32. The controller 11-1 then takes this video data into the GUI and supplies the video data, in the form of an NTSC signal, to the input terminal A of the DVCR 7-1.

Moreover, the controller 11-1 applies an infrared ray, thus transmitting a command which designates the video data to be output from the output terminal C of the DVCR 7-1 to a remote controller 12-1 connected to a serial port 31 by a dedicated serial cable 19-1. (The video data is either NTSC signal generated from the DV data supplied from the translator 10-1, or the NTSC signal supplied from the controller 11-1.)

The command, or the infrared-ray signal, output from the remote controller 12-1 is supplied to the DVCR 7-1. Upon receipt of the infrared ray at its light-receiving section 24 (FIG. 3), the DVRC 7-1 outputs the video data designated by the command, together with the audio data accompanying the video data, to the monitor 6-1 via an S-video cable 20-1 or a stereophonic audio cable 21-1. The monitor 6-1 displays the input video data, and the speaker (not shown) that is incorporated in the monitor reproduces the audio data.

The DVCR 7-1 can be controlled, without using the remote controller 12-1. It can be controlled by transmitting a control command may be transmitted via the IEEE1394 bus 5. Further, the remote controller 12-1 may be integrated with the controller 11-1.

Those of the components of the first network, which are shown in the right half

of FIG. 2, including the home router 4-2 and the remote controller 12-2, constitute a system for the other side of the TV telephone. They are of the same structure as the components shown in the left half of FIG. 2, including the home router 4-1 and the remote controller 12-1. Therefore, they will not be described.

The translator 10-1 and the controller 11-1 are connected by Ethernet (i.e., 10-base T cable 16-1). Nonetheless, they may be connected by the use of an optical fiber or an IEEE1394 bus, which can achieve IP connection. Since the translator 10-1 and the controller 11-1 are equivalent to the home router 4 shown in FIG. 1. Hence, the translator 10-1 and the controller 11-1 may be realized by one computer.

FIG. 5 depicts the configuration of the home router 4-1 comprising the translator 10-1 and the controller 11-1, which are integrated with each other. The CPU 41 reads a program stored in a memory 50, through a bus 51. The CPU 41 controls the entire home router 4-1 on the basis of the program. The IEEE1394 interface 42 is equivalent to the IEEE1394 card 21 shown in FIG. 3. The interface 42 is connected to the DVCR 7-1 and the DV camera 8-1 by IEEE1394 buses 5-1-1 and 5-1-2.

The video interface 43 is equivalent to the video card 33 shown in FIG. 4 and is connected to the DVCR 7-1 by S-video cables 17-1 and 17-2. The DVCR control interface 44 is equivalent to the serial port 31 shown in FIG. 4 and is connected to the remote controller 12-1 by the serial cable 19-1. The ATM interface 45 is equivalent to the ATM card 22 shown in FIG. 3 and transmits IP (Internet Protocol) data to the first network 1, after reserving a band or reserving no band. A mouse 47 and a

keyboard (not shown) are connected to the user input interface 46. A pointing device other than the mouse may be connected to the user input interface. The pointing device may be a touch panel, a track ball, or a voice recognition unit.

The hard disk interface 48 is connected to a hard disk 49. Stored on the hard disk 49 are programs, program-setting information, and the information hitherto input.

How the home router 4-1 performs data communication will be explained below, with reference to FIG. 6. The video signal and audio signal, which the DV camera 8-1 has generated, are converted to DV data (a DV packet). They are output, via the IEEE1394 bus 5-1-2, to the channel n (n is the channel number ranging from 0 to 53) that has been designated by the IEEE1394 interface 42. The IEEE1394 interface 42 receives the DV packet of the channel n at an IEEE1394 isochronous input cue 68-n. The DV packet supplied to the IEEE1394 isochronous input cue 68-n is transferred to and stored into the memory 50 under the control of the CPU 41.

The DV packets (A in FIG. 7) stored in a buffer 61 are put together, under the control of the CPU 41, making groups each consisting of one packet or more packets as is illustrated at B in FIG. 7. A sequential number is added the head of each packet group. Further, as is shown at C in FIG. 7, an IP header indicating the address of the destination (the other end of the line) is added to each packet group having the sequential number at the head, on the basis of the mapping table 63 stored in the memory 50 and designed for transmitting packets. The packet group is then converted to an IP packet.

09462342.040700

As shown at D in FIG. 7, the mapping table 62 stored in the memory 50 shows the numbers (0 to 63) of the channels in the IEEE1394 bus 5-1-2 (identical to the IEEE1394 bus 5-1-2) through which the DV data is transmitted from the DV camera 8-1. The table 62 also shows the IP addresses (i.e., addresses 0 to 63) of the home routers 4-2 of the destination that correspond to the channel numbers, respectively.

The table 62 also shows the numbers (i.e., the port numbers 0 to 63 of the home routers 4-2) of the channels in the IEEE1394 bus 5-2-1 (identical to the IEEE1394 bus 5-2-2) connected to the DVCR 7-2 of the destination.

The IP packet shown at C in FIG. 7 is transferred to the network output cue 63 of the ATM interface 49, under the control of the CPU 41. The IP data transferred to the network output cue 63 is output, by using the band the ATM interface 45 has reserved for the first network.

The IP packet transmitted from the other end of the line through the first network is stored into the network input cue 64 of the AMT interface 45. The IP packet stored in the network input cue 64 is transferred to the buffer 61 under the control of the CPU 41.

The CPU 41 refers to the sequential number of the IP packet (A in FIG. 8) transferred to the buffer 61, determining whether the packet has been lost or not. If the packet has been lost, the CPU 41 generates an IP packet to compensate for the packet lost.

The CPU 41 reads the IP header of the packet transferred to the buffer 61.

From the IP header or the mapping table 62 (D in FIG. 8), which is stored in the memory 50 and designed for transmitting packets, the CPU 41 determines the number m of the IEEE1394 bus 5-1-1 to which the IP packet will be output. (Here, m is the port number of the home router 4-1, or a port number 0, 1, 2, ... or 63.)

Further, the CPU 41 removes the IP header and the sequential number from the IP packet, as is illustrated at B in FIG. 8. The CPU 41 then divides the IP packet into DV packets, as is shown at C in FIG. 8.

The DV packets are transferred to the IEEE1394 isochronous output cue 66-m of the IEEE1394 interface 42 under the control of the CPU 41. (The cue 66-m corresponds to the channel of the IEEE1394 bus 6-1-1 connected to the DV terminal 25 of the DVCR 7-1.) If any DV packet contains timing information, the timing information will be supplied to an IEEE1394 output timing control section 65.

Under the control of the CPU 41, the DV packets are output from the IEEE1394 isochronous output cue 66-m to the channel m of the IEEE1394 bus 5-1-1 at the time represented by the timing information transmitted from the IEEE1394 output timing control section 65.

The communication initiated by an AV control command output from the home router 4-1 to the DVCR 7-1 or the DV camera 8-1 through the IEEE1394 bus 5-1 will be explained below. The AV control command for making the DV camera 8-1 to output DV data, for example, is generated in the buffer 61 under the control of the CPU 41. The AV command in the buffer 61 is transferred to the asynchronous output

cue 67 of the IEEE1394 interface 42. The AV command is output from the asynchronous output cue 67 to the IEEE1394 bus 5-1 under the control of CPU 41.

Meanwhile, the IEEE1394 interface 42 receives the response that the DV camera 7-1 has output upon receipt of the AV control command is output. This response is stored in an IEEE1394 asynchronous input cue 69. The response stored in the IEEE1394 asynchronous input cue 69 is transferred to the buffer 61 under the control of the CPU 41. The response is read to the CPU 41 thereafter.

As described above, a control signal can be supplied to the DVRC 7-1 via the IEEE1394 bus 5-1-1. It is also possible to supply the control signal from the remote controller 12-1, in the form of an infrared ray.

FIG. 9 shows a GUI which the CPU 41 has generated by executing the TV telephone application program stored in the hard disk 49 and which is displayed by the monitor 6-1. The GUI is so designed as to contain the image of the person at the other end of the line, whom a DV camera 8-2 has photographed under the control of the controller 11-1 (or the CPU 41). The GUI is input to the DVCR 7-1 from the video interface 43 through the S-video cable 17-1. The GUI is then supplied from the output terminal C of the DVCR 7-1 to the monitor 6-1.

The display section 71 of the GUI displays the image of the person at the other end of the line, which the DV camera 8-2 has photographed. The display section 72 of the GUI displays the connected time or a message indicating the communication state, such as "Contacting for connection."

A plurality of buttons are located on the right of the display sections 71 and 72. These buttons are operated by clicking the mouse 47. When a click at any of these buttons is input to the CPU 41 via the user input interface 46, the CPU 41 performs the process corresponding to the button operated. The user may operate the call button 73, for example, in order to transmit a connection request to the person whom the user wishes to talk with. In this case, a light spot moves from the left to the right in the call indicator 74, as is illustrated in FIG. 10A.

If that person at the other end of the line makes a call, a light potential will move from the right to the left in the call-waiting indicator 76 as is illustrated in FIG. 10B. This indicates that the connection request has been received.

To respond to the light spot (or call) moving in the call-waiting indicator 76, the user operates the catch button 75.

The user may operate the hang-up button 77 to release the connection. The user may set the monitor-on button 78 in the on state to make the display section 71 display the image of the person at the other end of the line as shown in FIG. 11B. Alternatively, the user may set the button 78 in the off state to make the display section 71 stop displaying the image of that person as shown in FIG. 11A.

The full-screen button 79 is operated to enlarge the image of the person, changing the size shown in FIG. 12A to the size shown in FIG. 12B and thus displaying the image on the entire screen of the monitor 6-1. The display-switching button 79 may be operated. When the user input interface 46 detects that the button 79 is

operated, the CPU 41 controls the remote controller 12-1 by way of the DVCR controller interface 44 and the dedicated serial cable 19-1. Thus controlled, the remote controller 12-1 transmits a command for switching the output of the DVCR 7-1, from the data (GUI) of the NTSC signal supplied from the controller 11-1 to the DV data supplied from the translator 10-1. When the mouse 47 is clicked in the state shown in FIG. 12B, the image on the monitor 6-1 is changed back to the GUI shown in FIG. 12A. That is, the remote controller 12-1 transmits a command to switch the output of the DVCR 7-1, when it is detected that the mouse 47 is operated.

The CPU 41 causes the monitor 6-1 to display such a setting input window as shown in FIG. 13, when the option button 80 is operated. The address, such as "192.168.1.2," of the home router 4-2 of the destination may be set, by using the IP address, the transfer address input section 91 of the setting input window. In the home router address input section 92, the address, such as "192.168.1.2," of the Ether card 23 that connects the translator 10-1 and the controller 11-1 is set by using the IP address. In the AMI net address, there is set, by using the IP address, the address, e.g., "192.168.2.1," (i.e., the address of the first network 1) of the ATM card 11 (or ATM interface 45) of the translator 10-1.

The size of the packet to be transmitted is set in the packet-size input section 94. The capacity of the buffer for received data is set in a receiving delay input section 95, in terms of the number of frames. If the capacity of the buffer is set at a large value, the display screen will be displayed in its entirety, but it will take a longer time to

0945234 - 040700

display the data. If the capacity is set at a small value, the data can be displayed within a shorter time, but some part of the image may not be displayed.

When the tick box 96 is ticked, it becomes possible to transmit both video information and audio information. Once the tick box 96 is de-ticked, it is possible to transmit the audio information only. When the tick box 97 is ticked, it becomes possible to receive both video information and audio information. Once the tick box 97 is de-ticked, it is possible to receive the audio information only. Usually the tick boxes 96 and 97 are ticked, whereby both the video information and the audio information can be transmitted and received.

When the remote-controller initiating button 98 is operated, the remote controller 12-1 is initiated. When the tick box 99 is ticked, it becomes possible to use the remote controller 12-1.

When the OK button 100 is operated, the various values set can be updated in accordance with the parameters input to the setting input window, and then the setting input window is closed. When the cancel button 101 is operated, the parameters input to the setting input window are invalidated, and the values set in the past are not updated, and then the setting input window is closed.

With reference to FIG. 9, the reset button 81 may be operated when the image of the person at the other end of the line is distorted or when a similar event takes places. When the reset button 81 is operated, the reception of information is interrupted, and the reception of video information is performed again. The end button

09452345 - 040700

82 is operated to terminate the TV telephone application.

The GUI of the TV telephone application is processed will be explained, with reference to the flow chart of FIGS. 14A to 14C. In Step S1, the CPU 41 determines whether the call button 73 has been pushed by operating the mouse 47. If it is determined that the call button 93 has been pushed, the operation goes to Step S2 (FIG. 14B). In Step S2, the CPU 41 outputs a connection request to the first network via the ATM interface 5, in accordance with the information set in the setting input window.

In Step S3, the CPU 41 determines whether or not the ATM interface 45 has received via the first network the response to the connection request, which is supplied from the destination (i.e., the person the user wishes to talk with). If it is determined in Step S3 that the ATM interface 45 has not received the response to the connection request, the operation goes to Step S4. In Step S4, the CPU 41 determines whether or not a prescribed time has elapsed after the transmission of the connection request. If the CPU 41 determines that the prescribed time has not elapsed, the operation returns to Step S3, whereby the response to the connection request is waited for. If the CPU 41 determines, in Step S4, that the prescribed time has elapsed, the operation returns to Step S1.

If the CPU 41 determines, in Step S3, that the response to the connection request has been received, the operation goes to Step S5. In Step S5, the CPU 41 stores, into the memory 50, the AMI net IP address and port number of the destination, which are contained in the response received. Then, in Step S6, the CPU 41 makes the

ATM interface 46 reserve a band for the first network. In Step S7, the CPU 41 determines whether or not a band for the first network has been reserved successfully. If the CPU 41 determines that the band has been reserved successfully, the operation goes to Step S8.

In Step S8, the CPU 41 determines whether or not the memory 50 stores the values set for transmitting data to the destination (i.e., the mapping table 62 shown at D in FIG. 7). If the CPU 41 determines that the memory 50 does not store the values set for transmitting data to the destination, the operation goes to Step S9. In Step S9, the CPU 41 generates a mapping table which shows the number of the IEEE1394 channel the DV camera 8-1 will use and the AMI net IP address and port number of the destination, which correspond to the channel number. The mapping table is stored into the memory 50. If it is determined in Step S8 that the memory 50 stores the values set for transmitting data to the destination, the operation will skip Step S9 since the values set for transmitting data are utilized.

In Step S10, the CPU 41 transmits an AV control command to the DV camera 8-1 via the IEEE1394 to output DV data (video data and audio data) to the IEEE1394 channel designated. The ATM interface 45 converts the DV data to IP data, which is output to the first network.

In step S11, the CPU 41 determines whether or not the memory 50 stores the values set for receiving data from the destination (i.e., the mapping table 62 shown at D in FIG. 8). If it is determined that the memory 50 does not store the values set for

receiving data from the destination, the operation goes to Step S12. In Step S12, the CPU 41 generates a mapping table (D in FIG. 8) which shows the IP address of the home router 4-2 of the destination and that channel of the IEEE1394 bus 5-1 which is connected to the DVCR 7-1. This mapping table is stored into the memory 50. If it is determined in Step S11 that the memory 50 stores the values set for receiving data from the destination, the operation will skip Step S12 since the values set for receiving data are utilized.

In Step S13, the CPU 41 initiates the process of receiving data. The data-receiving process will be explained in detail, with reference to the flow chart of FIG. 15. In Step S51, the ATM interface 45 receives an IP packet from the first network under the control of the CPU 41. The IP packet is recorded in the network input cue 64 and then transferred to the buffer 61. The CPU 41 reads the values (mapping table 62 shown at D in FIG. 8) set for receiving data and stored in the memory 50, thereby determining a channel for outputting the IP packet.

In Step S52, the CPU 41 extracts a DV packet from the IP packet stored in the buffer 61. The DV packet is transferred to the IEEE1394 isochronous output cue 66-m of the IEEE1394 interface 42.

In Step S53, the CPU 41 determines whether the DV packet, which has been extracted in Step S52, contains timing information or not. If it is determined that the DV packet contains no timing information, the operation returns to Step S52. Thus, another DV packet is extracted and transferred. If it is determined that the DV packet

0945234-040700

contains timing information, the timing information is supplied to the isochronous output timing control section 65.

In Step S54, the IEEE1394 interface 42 waits until the isochronous output timing control section 65 instructs that the process of outputting data be started. When the section 65 instructs the start of data-outputting, the operation goes to Step S55.

In step S55, the IEEE1394 interface 42 outputs the DV data from the IEEE1394 isochronous output cue 66 to the IEEE1394 bus 5-1, at the timing designated by the isochronous output timing control section 65.

The DV data (video data and audio data) is input to the DVCR 7-1 through the IEEE1394 bus 5-1. The audio data is supplied, not modified, to the monitor 6-1 and reproduced by the monitor 6-1. The video data is incorporated into the GUI in the DVCR 7-1. The GUI is supplied to the monitor 6-1 and displayed by the monitor 6-1.

In Step S14 (FIG. 14C), the CPU 41 determines whether or not the hang-up button 77 has been pushed. If it is determined that the hang-up button 77 has not been pushed, the operation goes to Step S15. In Step S15, the CPU 41 determines whether or not the ATM interface 45 has received an end-of-talk message from the other end of the line. If it is determined that the ATM interface 45 has not received the message, the operation goes to Step S16.

In Step S16, the CPU 41 determines whether the monitor-on button 78 has been pushed or not. If it is determined that the monitor-on button 78 has been pushed, the operation goes to Step S17. In Step S17, the CPU 41 causes the display section 71 to

0546234.040400

delete the image of the person at the other end of the line, if the section 71 has been displaying the image, or to display the image if the section 71 has not displayed the image. Thereafter, the operation returns to Step S14.

If it is determined in Step S16 that the monitor-on button 78 has not been pushed, the operation goes to Step S18. In Step S18, the CPU 41 determines whether the display-switching button 79 has been pushed or not. If it is determined that the display-switching button 79 has been pushed, the operation goes to Step S19. In Step S19, the CPU 41 causes the remote controller 12-1 to transmit a command, whereby the output of the DV 7-1 is switched to the DV data supplied from the translator 10-1. As a result, the monitor 6-1 displays the DV data on its entire screen, as is illustrated in FIG. 12B.

In Step S20, the CPU 41 remains to perform any process until the mouse 47 is clicked. If the CPU 41 determines in Step S20 that the mouse 47 has been clicked, it transmits a command to the remote controller 12-1 in Step S21. In response to the command, the remote controller 12-1 switches the output of the DVCR 7-1 to the GUI supplied from the controller 10-1. As a result, the monitor 6-1 displays the GUI as is illustrated in FIG. 12A. Thereafter, the operation returns to Step S14.

If it is determined in Step S18 that the full-screen button 79 has not been pushed, the operation goes to Step S22. In Step S22, the CPU 41 determines whether the reset button 81 has been pushed or not. If it is determined that the reset button 81 has been pushed, the operation goes to Step S23. In Step S23, the CPU 41 controls the

09452342 - 040900

ATM interface 45, causing the interface 45 to stop receiving data from the first network. In Step S24, the CPU 41 again performs the process of receiving data (similar to the process carried out in Step S13).

If it is determined in Step S22 that the reset button 81 has not been pushed, the operation returns to Step S14.

It may be determined in Step S14 that the hang-up button 77 has been pushed, it may be determined in Step S15 that the end-of-talk message has been transmitted from the other end of the line. Further, it may be determined in Step S7 that a band for the first network has not been reserved successfully. If this is the case, the operation will go to Step S25. In Step S25, the CPU 41 informs the destination of the termination of connection. In Step S26, the CPU 41 controls the ATM interface 45, causing the same to stop transmitting the IP packet to the first network. The CPU 41 also transmits an AV control command to the DV camera 8-1 via the IEEE1394 interface 42, thereby making the DV camera 8-1 stop outputting the DV data.

In Step S27, the CPU 41 erases from the memory 60 the transmission mapping table 62 (D in FIG. 7) showing the number of the IEEE1394 channel, which the DV camera 8-1 has used, and the AMInetIP address and port number of the destination.

In Step S28, the CPU 41 controls the ATM interface 45, causing the same to cancel the band reserved for the first network.

In Step S29, the CPU 41 controls the ATM interface 45, causing the same to stop receiving data from the first network.

In Step S30, the CPU 41 erases from the memory 50 the receiving mapping table 62 (D in FIG. 8) showing the IP address of the home router 4-2 of the destination and the channel m of the IEEE1394 bus to which the DVCR 7-1 is connected. Thereafter, the operation returns to Step S1.

With reference to FIG. 14A again, if it is determined in Step S1 that the call button 73 has not been pushed, the operation goes to Step S31. In Step S31, the CPU 41 determines whether the option button 80 has been pushed or not. If it is determined that the option button 80 has been pushed, the operation goes to Step S32. In Step S32, the CPU 41 makes the monitor 6-1 display the setting input window shown in FIG. 13. The user inputs various values into the window. The operation then returns to Step S1.

If it is determined in Step S31 that the option button 80 has not been pushed, the operation goes to Step S33. In Step S33, the CPU 41 determines whether a call has arrived from any other user or not (that is, whether the ATM interface 45 has received a connection request or not). If it is determined that no call has arrived, the operation goes to Step S34. In Step S34, the CPU 41 determines whether the end button 82 has been pushed or not. If it is determined that the end button 82 has not been pushed, the operation returns to Step S1. If it is determined that end button 82 has been pushed, the CPU 41 terminates the GUI process (the TV telephone application).

If it is determined in Step S33 that a call has arrived, the operation goes to Step S35. In Step S35, the CPU 41 determines whether the catch button 75 has been pushed

0054529.0004

or not. If it is determined that the catch button 75 has not been pushed, the operation goes to Step S36. In Step S36, the CPU 41 determines whether a prescribed time has elapsed after the arrival of the call. If the prescribed time has not elapsed, the operation returns to Step S35. The CPU 41 remains to perform any process until the catch button 75 is pushed. If it is determined in Step S46 that the prescribed time has elapsed, the operation returns to Step S1.

If it is determined in Step S35 that the catch button 75 has been pushed, the operation goes to Step S37. In Step S37, the CPU 41 stores the IP address that is contained in the call (i.e., connection request), into the memory 50. Further, the CPU 41 outputs a response to the call, i.e., the channel number n of the IEEE1394 bus 5-1, to which the DV camera 8-1 is connected, and the address of the home router 4-1. The response is output through the ATM interface 45. Thereafter, the operation goes to Step S6, whereby the steps following Step S6 are carried out.

In the present embodiment, the DV data (image, voice and sound) the DV camera 8 has generated is communicated in real time as described above. The so-called "TV telephone" can be therefore realized. In addition, it is possible with this embodiment to communicate the DV the DVCR 7 has reproduced from magnetic tape.

In transferring data in the isochronous mode through the IEEE1394 bus 5, the timing of transmitting each data packet has a tolerance of only hundreds of microseconds. This is a considerably strict condition for software that operates on the non-real-time operating system (OS).

0960204-0960204

In the process of transferring the video data generated by the DV camera operating on the IEEE1394 bus 5-1-2 to the DVCR 7-2 operating on the IEEE1394 bus 5-2-1 through the first network, the lag between the clock signals on the buses 5-1-2 and 5-2-1 may accumulate. (This may take place also in the process of transferring the vide data generated by the DV camera 8-2 operating on the IEEE1394 bus 5-2-2 to the DVCR 7-1 operating on the IEEE1394 bus 5-1-1.) As a consequence, the buffer 61 may overflow or underflow. A method of preventing such overflow and overflow will be described below.

The principle of the method will be explained at first. Assume that the image photographed by the DV camera 8-2 is transmitted to the DVCR 7-1. The application controlling the transfer on the OS of the CPU 41 writes the data generated by the DV camera 8-2, into the isochronous output cue 66. This data includes the isochronous packet header written from the network input cue 64 to the buffer 61. After hundreds of data packets have been written into the isochronous output cue 66, the application explicitly instructs the device driver for the isochronous output cue 66 to start transmitting the packets. When the start of transmitting packets is instructed, it is possible to designate the bus cycle at which the transmission of packets should be started. Once the transmission of packets is started, the data is continuously transmitted. Hence, the application must keep writing the data.

To reduce the load on the CPU 41, the device driver makes the buffer 61 store hundreds of data packets or thousands of data packets and chains the DMA. Hence,

hundreds of data packets can be transmitted at a single interruption. Thanks to this, even with a non-real-time OS it is possible to transmit a packet in each of the 8,000 isochronous cycles per second (that is to say, in a cycle of 125 microseconds).

The data is transmitted through the IEEE1394 bus 5-1-1, at the rate of one packet per isochronous cycle. A packet may not be transmitted due to DMA transfer error or any other error. If this happens, the device driver will discard the data stored in the buffer 61, thereby transmitting packets in the same number of cycles. This process is effected by making an interruption after the completion of the DMA transfer. Therefore, a temporal displacement between each cycle and the packet may occur. Nonetheless, since data is discarded from the buffer 61, the displacement will be eliminated upon lapse of a predetermined period (or after about two interruptions are made by the DMA). This period depends on the number of interruptions the DMA makes, not on the buffer size of the device driver. Hence, the period can be a relatively short.

Since the bus cycle is designated at the start of transmitting packets and is duly made to correspond to the data, the applicant can accurately determine the timing of actually transmitting the data (to be written) to the IEEE1394 bus 5-1-1. In addition to this, the isochronous output cue 66 used as a memory to transfer isochronous packets is of FIFO configuration. Therefore, it is possible to control the timing of each isochronous packet in the application process having low real-time degree.

With reference to the flow chart of FIG. 16 it will be explained how the

0945345 - 040900

application working in the CPU 41 transmits an isochronous packet. In Step S71, the CPU 41 (or the application) extracts a packet from the network input cue 64. In Step S72, the CPU 41 determines whether or not the packet extracted contains a time stamp. A packet having a time stamp has the configuration shown in FIG. 17. SYT in FIG. 17 is the time stamp. A packet that has no time stamp has the configuration shown in FIG. 18. The values in the time stamp field (i.e., the field of SYT) are all "1s."

In the packets shown in FIGS. 17 and 18, "Data length" is the length of the packet, and "Tag" indicates the format label of the isochronous packet. "Channel" is means the number (any one of 0 to 63) of the channel in the IEEE1394 bus 5. "Tcode" means the type of the packet and also the type of the transaction. In the case of isochronous data, Tcode is set at the value of "10."

"Sy" stands for a synchronization code for achieving the control specific to the application. "Header CRC (Cyclic Redundancy Check)" indicates a code for detecting an error in a header. That is, this code describes the CRC of Data length, Tag, Channel and Sy. "SID" means a source node ID, i.e., the node number of the source of the packet. "DBS" stands for data block size.

"FN (function number)" is the number of a function. "QPC (Quadlet padding count) indicates the number of paddings. "SPH (source packet header)" indicates whether or not the data contains a source packet header. "DBC (Data block count)" indicates the sequential number of a data block. "FMT" is the format number used; it is "0" for digital video information. And "FDF (Format dependent data) is the

0054345.0100

information specific to the format.

According to IEC61883-1, the time stamp and bus cycle of the CIP header must correspond to each other. The lag between the time stamp and the bus cycle has a tolerance of only a few cycles. (Empirically, the tolerance ranges from 0 cycle to 1 cycle only.) Hereinafter, the value of the time stamp of the CIP header shall be called "timing of the packet," whenever necessary. In the case of DVC, there exist packets having no time stamps. The timing of such a packet is determined from the timing of a packet having a time stamp, by means of simple linear interpolation.

If it is determined in Step S72 that the packet contains a time stamp, the operation goes to Step S73, in which the variable n representing the number of packets is incremented by one. The variable n will be reset to "0" in Step S80, at the timing of changing the data rate.

Next, in Step S74, the CPU 41 adds the amount of data held in the isochronous output cue 66 to the variable S that represents the amount of data accumulated in the isochronous output cue 66. In Step S75 the CPU 41 multiplies the time stamp of the packet by the rate R, thereby correcting the time stamp.

If it is determined in Step S72 that the packet does not contain a time stamp, the operation jumps to Step S76, skipping Steps S73 to S75.

In Step S76, the CPU 41 inserts the packet into the output cue 66 and adds the amount of data (packet) to the variable N that represents the data which has been accumulated in the cue 66 and which is to be transmitted. In Step S77, the CPU 41

09452342.010700

determines whether the variable n incremented in Step S73 has reached a predetermined value (e.g., 100) or not. That is, it is determined whether the time has come to change the rate R. If the value of n has not reached 100, the operation returns to Step S71, and Step S71 et seq. are then repeatedly performed.

If it is determined in Step S77 that the value of n has reached 100 (that is, if it is determined that the time has come to change the rate R), the operation goes to Step S78. In Step S78, the CPU 41 calculates a new rate R from the average data amount A (= S/n) in the isochronous output cue 66, the accumulated amount of data to transmit, and the current rate R. Further, in Step S79, the CPU 41 holds the average data amount A in preparation for the next calculation, and clears the value S representing the amount of data in the isochronous output cue 66 and the accumulated amount N of data to be transmitted. In other word, the values of S and the value of N are changed to "0." Then, in Step S80, the CPU 41 resets the variable n to the value of "0." Thereafter, the operation returns to Step S71, and Step S71 et seq. are repeatedly performed.

Step S76 of inserting the packet into the output cue 66 and adding the amount of data thereof to the amount of data to be transmitted will be explained in detail, with reference to the flow chart of FIG. 19. In Step S91, the CPU 41 determines whether the packet contains a time stamp or not. If the packet contains no time stamp, a time stamp (timing) is calculated by means of linear interpolation. If it is determined in Step S91 that the packet contains a time stamp, the CPU 41 determines in Step S93

whether or not the time stamp (timing) is greater than the sum (VCt + D) of the count VCt of a cycle counter, indicating the bus cycle, and a constant D determined from the delay caused by transfer, if the time stamp (timing) has been calculated in Step S92 by linear interpolation.

That is to say, it is determined whether the time has come to output the packet. If the time stamp the packet contains is equal to the sum of the count VCt and the constant D or is less than the sum, the time has not come to output the packet. In this case, the operation goes to Step S94. In Step S94, the CPU 41 inserts an empty packet into the isochronous output cue 66 and adds a value C to the count VCt. The value C indicates a one-cycle length. Then, the operation returns to Step S93, and the value of the time stamp is compared again with the sum of the count VCt and the constant D.

FIG. 20 shows the format of the empty packet to be inserted into the isochronous output cue 66. As shown in this figure, the data is all "1s."

Since the number of times the data is written is duly made to correspond to the bus cycle for outputting the data, as described above, the CPU 41 can easily determine the cycle in which to output the data to be written is output to the bus, by increasing the count VCt by one every time the function write() is executed to write the data. The CPU 41 compares this virtual cycle with the timing of each packet, thereby determining the timing of transmitting the packet.

In the program actually used, any packet having no time stamp may be stored into a buffer, without executing the function write(), the timing for the packet stored

in the buffer may be obtained when a packet having a time stamp is written, and the function write() may then be executed. As a result of this, the timing for each packet can be calculated by means of linear interpolation. Since the smallest unit for the time stamp of the CIP header is 1/(12 × 256) cycle, the count VCt and the one-cycle length C are calculated, also in units of 1/(12 × 256) cycles.

If it is determined in Step S93 that the time stamp (timing) is greater than the sum of the count VCt and the constant D, the operation goes to Step S95. In Step S95, the CPU 41 inserts the packet into the isochronous output cue 66, adds the value C, i.e., one-cycle length, to the count VCt, and adds the amount of data, which is then being transmitted, to the accumulate amount N. The operation then goes to Step S96, in which the CPU 41 determines whether the transmission has been started or not. If the transmission has not been started, the operation goes to Step S97. In Step S97, the CPU 41 determines whether the isochronous output cue 66 holds a sufficiently large packet or not. If the isochronous output cue 66 holds a sufficiently large packet, the operation goes to Step S98, in which the CPU 41 starts the transmission. If the isochronous output cue 66 does not hold a sufficiently large packet, Step S98, the start of transmission, is skipped.

As described above, the CPU 41 indirectly infers the lag between the clock signal on the IEEE1394 bus 5-2-2 and the clock signal on the IEEE1394 bus 5-1-1, from the amount of data held in the isochronous output cue 66. The device driver has a function ioctl() for supplying data from the driver in units of bytes. This function

ioctl() can be obtained in accurate value, along with the amount of data stored in a software buffer, from the state of the DMA register and in consideration of the condition in which the DMA is being executed.

The application monitors the amount of data at suitable intervals, a plurality of times, and repeatedly obtain the average amount of data. It compares the average amount of data with the average amount obtained last, thereby detecting whether or not the data has increased or decreased. It is therefore possible to determine the lag between the clock signal on the bus of the source and the clock signal on the bus of the destination. Good results can be attained even if the sampling intervals differ from each other, provided that the sampling frequency is increased to some extent. Theoretically, the data can be sampled at random.

The lag between the clock signals can be calculated, only by storing the amount of data written in accordance with the system call of the function write(). The average amount of data, monitored last, may be 500KB, and the average amount of data, monitored at present, may be 501KB. If so, the lag between the clock signals is calculated as follows, provided that 1000MB has been written since the last monitoring of the average amount of data:

(501KB - 500KB)/1000MB = 0.000001

In this case, the interval between the clock pulses on the IEEE1394 bus 5-2-2 of the source is shorter by about 1 p.p.m. (parts per million).

The rate R is defined so as to inhibit the increase or decrease in the amount of

data stored in the isochronous output cue 66.

The rate R is, for example, 1.00001, almost equal to 1.

The timing Pt(i) of a packet P(i) (i = 0, 1, 2, ... n) captured is corrected to Pt'(i), as is expressed by the following equation:

$$Pt'(i) = Ct0 + (Pt(i) - Ct0) \times R$$
$$= Ct0 + (Pt(i) - Ct0) \times Rc/Rm$$
$$= Pt'(i - 1) + (Pt(i) - Pt(i-1) \times Rc/Rm$$

In this equation, R = Rc/Rm, and Rc, and Rm are two integers. Rm is fixed at 1000000 and Rc is changed, thereby defining the rate R. If data is transmitted for a long time, Pt(i) - Ct0 will increase very much. This is why Pt'(i - 1) is used in place of Ct(0) in the above equation.

The data stored in the isochronous output cue 66 will be transmitted fast if the value for R is decreased, and slowly if the value for R is decreased. The rate R may be set an appropriate value, thereby to compensate for the lag between the clock signals on the two buses. The data held in the buffer can therefore remain unchanged.

In order to reduce the error further, the remainder of integer division, Rest(i), may be stored so as to be used in the next calculation. If so, the timing Pt'(i) corrected by applying the rate R will be given as follows:

$$Pt'(i) = Pt'(i -1) + ((Pt(i) - Pt(i-1))$$
$$\times Rc + Rest(i -1)/Rm$$

Here, Rest(i) is expressed by the following equation:

$$Rest(i) = ((Pt(i) - Pt(i-1) \times Rc + Rest(i-1)$$

$$-((Pt(i) - Pt(i-1)) \times Rc + Rest(i-1))/Rm \times Rm$$

If B is substitute for $((Pt(i) - Pt(i-1) \times Rc + Rest(i-1)$, the equation will reduce to the following:

$$Rest(i) = B - (B/Rm) \times Rm$$

Algebraically, the value for $(B/Rm) \times Rm$ is B. When an integer operation is performed, however, the value differs from B due to rounding error in the division and becomes Rest(i).

The average amount A' of data stored in the isochronous output cue 66 may be calculated again after the average amount A of the data in the isochronous output cue 66 is obtained and the data is then output for a predetermined period. In this case, the rate R' for eliminating the lag between the clock signals is obtained as follows:

$$R' = (N/(N + A' - A) \times R$$

where N is the amount of all data processed during that period by the function write(), and R is the rate at which the data is transmitted.

This equation has been formulated by the inventors hereof and has not been certified as true. Empirically, however, the equation is sufficiently valid.

Moreover, in order to maintain the amount of data in the isochronous output cue 66 at a prescribed value A, the rate R' may be further corrected to rate R", as indicated below, and this rate R" may be applied:

$$R'' = R' - (A - A0)/A0 \times F$$

where F is a constant which ranges from 1/1000 to 1/100000.

Isochronous packets are transmitted, usually by means of a dedicated link chip. The format of them is one suitable for use in AV apparatuses and the like. If the control system according to this invention is used, however, data streams can be controlled by general-purpose hardware and OS.

It is expected that personal computers will soon incorporate a standard host adapter having the common-standard IEEE1394 link chip called "1394OHCI (1394 0pen Host Controller Interface). Since the OHCI specification is based on PELE, such a control method as used in the present invention will be effective.

Mainly the DVC format has been explained above. Nevertheless, many things described above do not depend on the format. Hence, this invention can be applied to other formats, as well.

0546254 - 040700